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by Razavi, B.;

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## » Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

- ☐ **1. Design self-synchronized clock distribution networks in an SoC ASIC using remote clock feedback**  
Hyun Lee; Han Quang Nguyen; Potter, D.W.;  
[ASIC/SOC Conference, 2000. Proceedings, 13th Annual IEEE International](#)  
13-16 Sept. 2000 Page(s):248 - 252  
Digital Object Identifier 10.1109/ASIC.2000.880710  
[AbstractPlus](#) | Full Text: [PDF](#)(320 KB) [IEEE CNF](#)  
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- ☐ **2. Novel broad-band bit-synchronization circuit module for optical interconnect**  
Onodera, K.;  
[Microwave Theory and Techniques, IEEE Transactions on](#)  
Volume 52, Issue 2, Feb. 2004 Page(s):475 - 481  
Digital Object Identifier 10.1109/TMTT.2003.821921  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(808 KB) [IEEE JNL](#)  
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- ☐ **3. Time borrowing and clock skew scheduling effects on multi-phase level-shifters**  
Taskin, B.; Kourtev, I.S.;  
[Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International](#)  
Volume 2, 23-26 May 2004 Page(s):11 - 617-20 Vol.2  
[AbstractPlus](#) | Full Text: [PDF](#)(270 KB) [IEEE CNF](#)  
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- ☐ **4. Operation of a 1-bit quantum flux parametron shift register (latch) by 4-phase clock**  
Hosoya, M.; Hioe, W.; Takagi, K.; Goto, E.;  
[Applied Superconductivity, IEEE Transactions on](#)  
Volume 5, Issue 2, Part 3, Jun 1995 Page(s):2831 - 2834  
Digital Object Identifier 10.1109/77.403181  
[AbstractPlus](#) | Full Text: [PDF](#)(324 KB) [IEEE JNL](#)  
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- ☐ **5. A dynamic clock synchronization technique for large systems**  
Brueske, D.E.; Embabi, S.H.K.;  
[Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging Technology, IEEE Transactions on](#)  
[see also [Components, Hybrids, and Manufacturing Technology, IEEE Transactions on](#)]



emulation + clock synchronization circuit

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### Circuit emulation services over Ethernet—Part 1: Clock synchronization using timestamps - group of 2 »

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J Aweya, M Ouellette, DY Montuno, K Felske - International Journal of Network Management, 2004 - doi.wiley.com

... This technique, known as **circuit emulation**, must address issues of network delay, jitter and **clock synchronization** to handle TDM traffic properly. ...

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### Pausable clocking-based heterogeneous systems - group of 5 »

KY Yun, AE Dooply - Very Large Scale Integration (VLSI) Systems, IEEE ..., 1999 - [ieeexplore.ieee.org](#)

... A. **Synchronization** Strategy A block diagram of the PCC is ... separation of the sampling edges of the **clock** and external ... An ME [2], [8] is a **circuit** that allows ...

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### Source synchronization and timing Vernier techniques for 1.2 GB/s SDRAM interface - group of 2 »

Y Morooka, Y Nakase, JM Choi, HJ Shin, DJ Perlman, ... - Solid-State Circuits Conference, 1998. Digest of Technical ..., 1998 - [ieeexplore.ieee.org](#)

... by the SDRAM interface chip with source **synchronization** and timing ... Figure 3 Source synchronized input/output scheme (a) **Clock** distribution and ... **emulation** ...

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### Boundary-scan: beyond production test

RM Sedmark - VLSI Test Symposium, 1994. Proceedings., 12th IEEE, 1994 - [ieeexplore.ieee.org](#)

... **Clock synchronization** problems between the system **clock** and TCK ... 2.1.4 Benefits of Boundary-Scan **Emulation** and Logic Analysis Based The benefits of boundary ...

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### ATM circuit emulation-a comparison of recent techniques

KM Ahmed, MG Hluchyj - Global Telecommunications Conference, 1991. GLOBECOM'91. ..., 1991 - [ieeexplore.ieee.org](#)

Page 1 0370 CH2980-119110000-0370 \$1.00 © 1991 IEEE GLOBECOM '91 **ATM Circuit Emulation** - A Comparison of Recent Techniques Hassan M. Ahmed Boston University ...

Cited by 6 - [Web Search](#)

### Virtual in-circuit emulation for timing accurate system prototyping

L Benini, D Bruni, N Drago, F Fummi, M Poncino - ASIC/SOC Conference, 2002. 15th Annual IEEE International, 2002 - [ieeexplore.ieee.org](#)

... Figure 2: Virtual In-Circuit **Emulation** Scheme. ... is showed in Figure 6. Timing **synchronization** is implemented by ... computes the exact number of **clock** cycles used ...

Cited by 4 - [Web Search](#)

### A transaction-based unified simulation/emulation architecture for functional verification - group of 9 »

M Kudlugi, S Hassoun, C Selvidge, D Pryor - Design Automation Conference, 2001. Proceedings, 2001 - [ieeexplore.ieee.org](#)

... When synchronizing a C simulation with **emulation**, the C ... to forge ahead, performing one or more **clock** cycles worth of work after each **synchronization** point ...

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